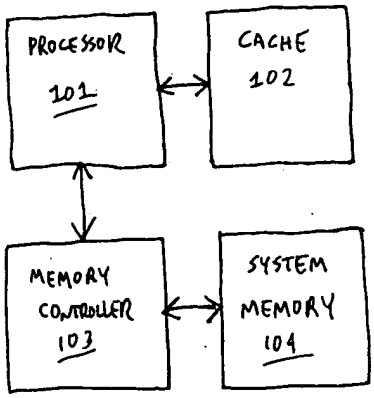


FIG. 1
(PRIOR ART)

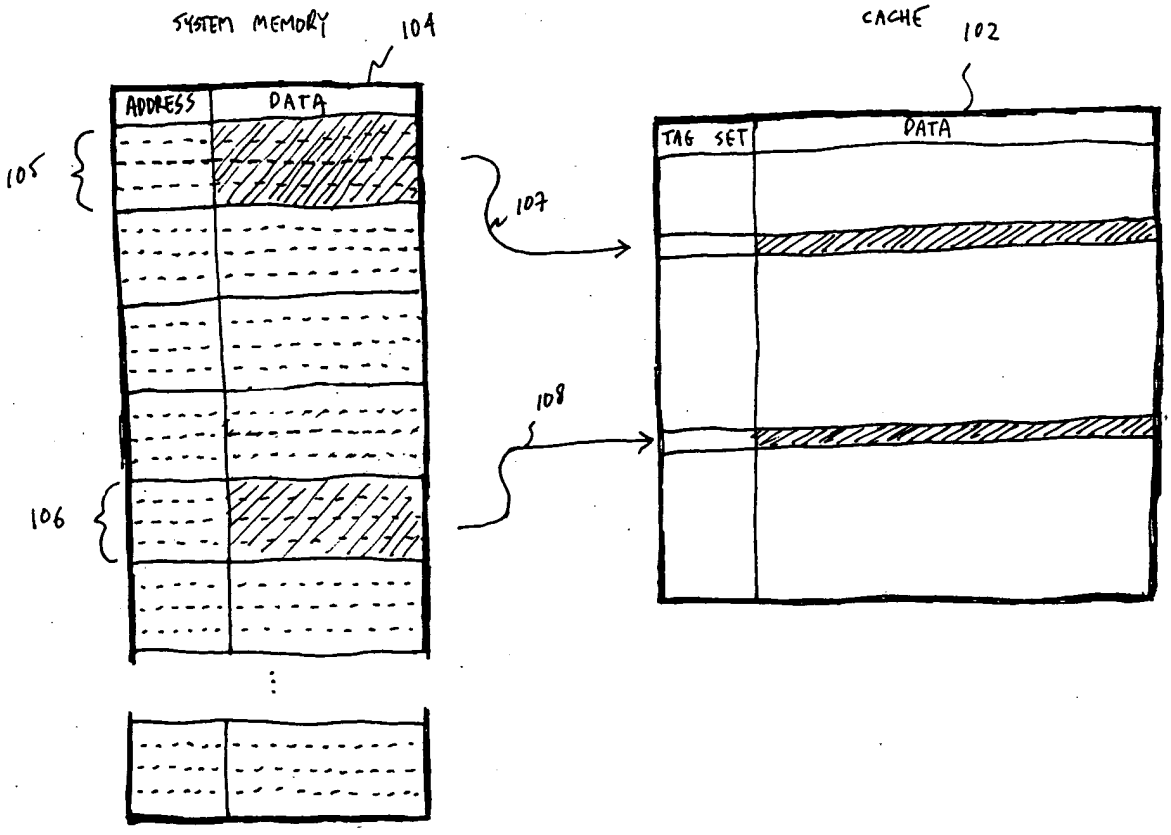


FIG. 2
(PRIOR ART)

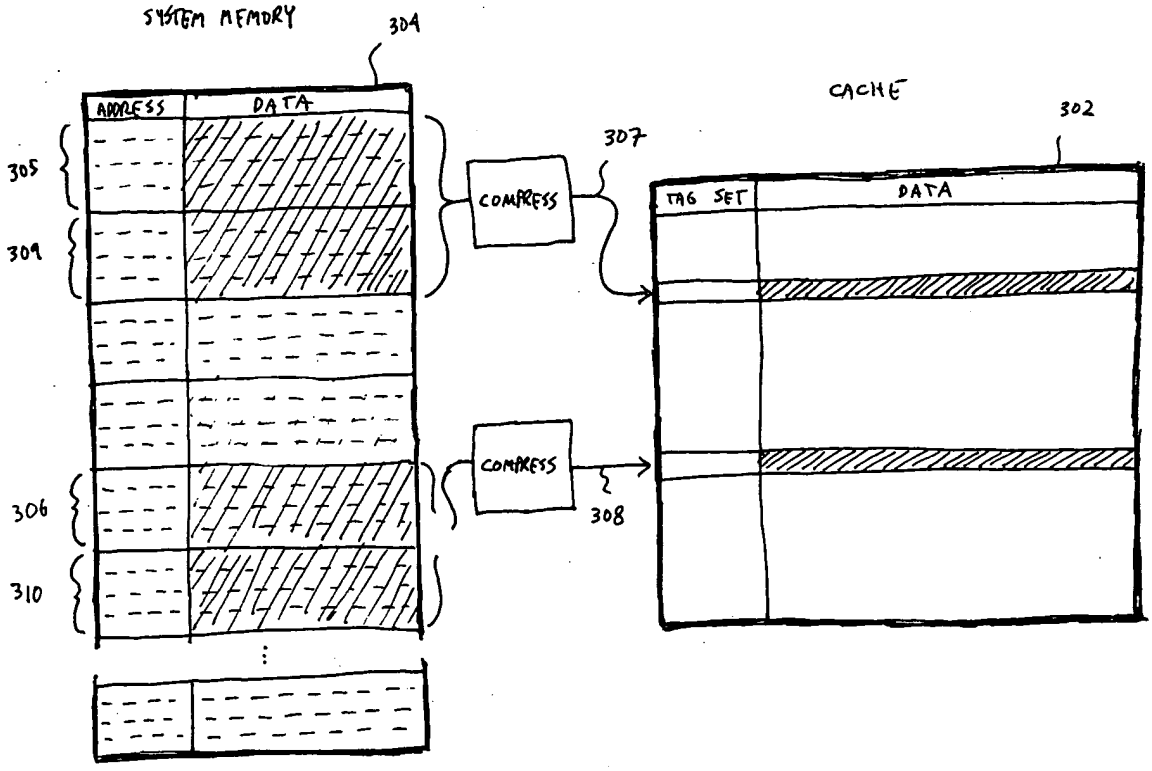

SYSTEM MEMORY
304
ADDRESS
DATA
305
309
306
310
COMPRESS
COMPRESS
307
308
CACHE
302
TAG SET
DATA

FIG. 3A

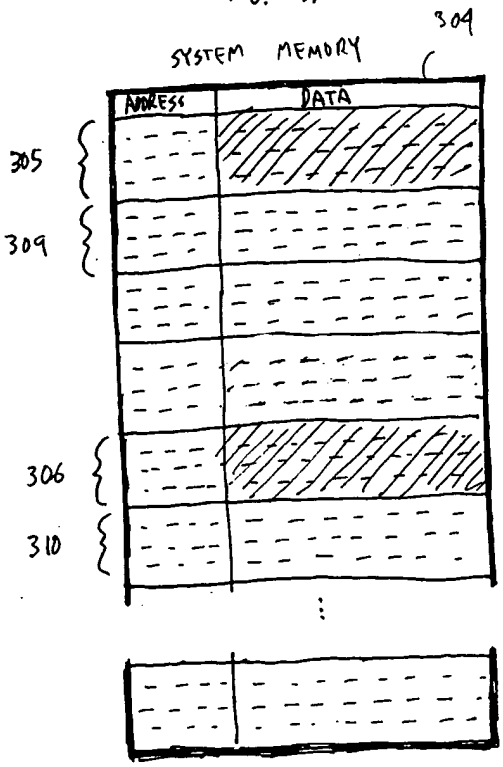

304
SYSTEM MEMORY
ADDRESS
DATA
305
309
306
310

FIG. 3B

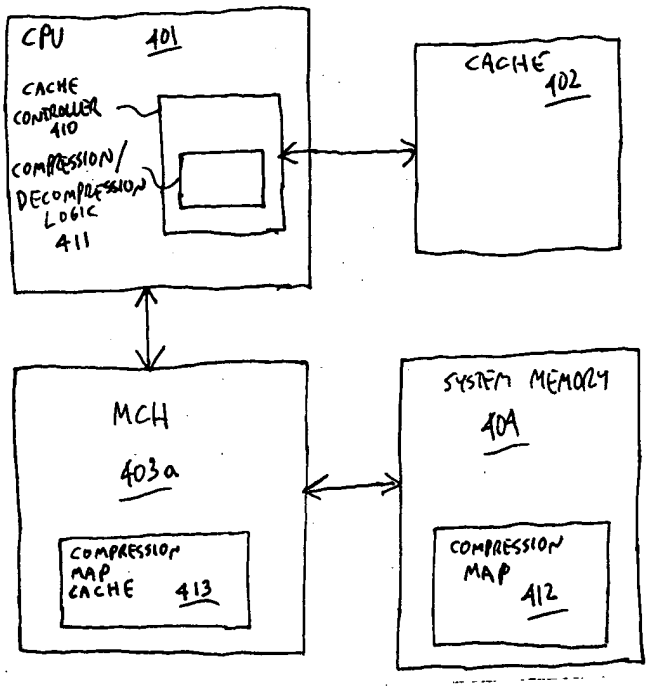

CPU
101
CACHE CONTROLLER 410
COMPRESSION/ DECOMPRESSION LOGIC 411
CACHE
102
MCH
403a
COMPRESSION MAP CACHE 413
SYSTEM MEMORY
404
COMPRESSION MAP 412

FIG. 4A

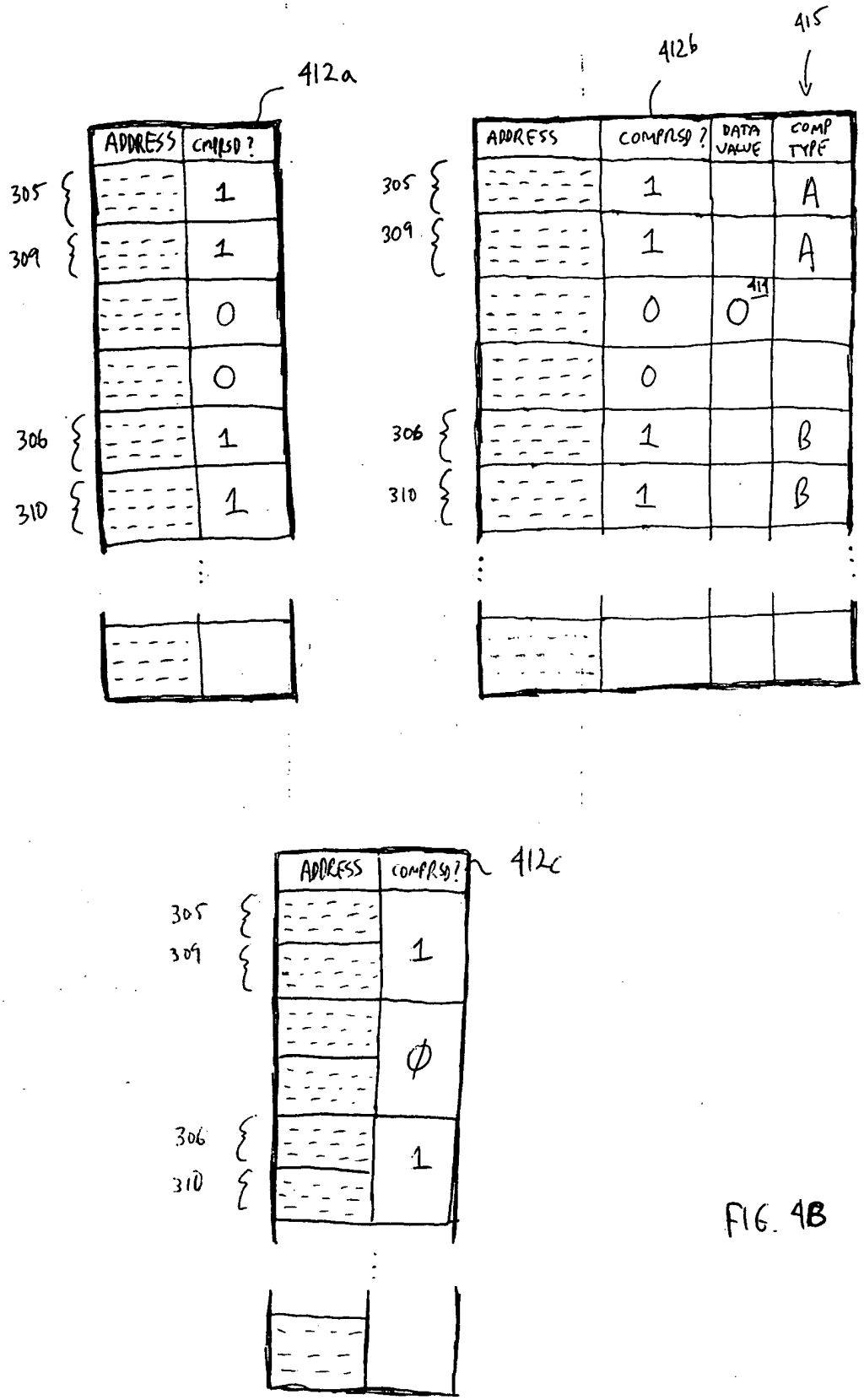

412a
ADDRESS
CMPRSD?
305
309
306
310
1
1
0
0
1
1
412b
415
ADDRESS
COMPRSD?
DATA VALUE
COMP TYPE
305
309
306
310
1
1
0
0
1
1
419
A
A
B
B
412c
ADDRESS
COMPRSD?
305
309
306
310
1
ϕ
1

FIG. 4B

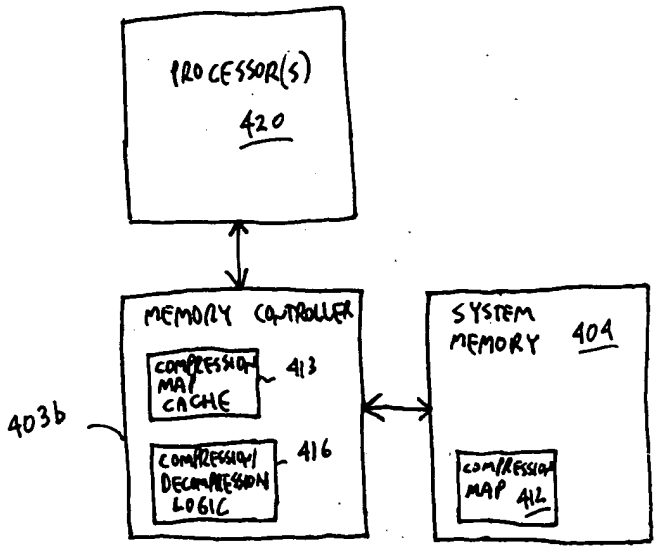

PROCESSOR(S)
420
MEMORY CONTROLLER
COMPRESSION MAP CACHE
413
403b
COMPRESSION/ DECOMPRESSION LOGIC
416
SYSTEM MEMORY
404
COMPRESSION MAP 412

FIG. 4C

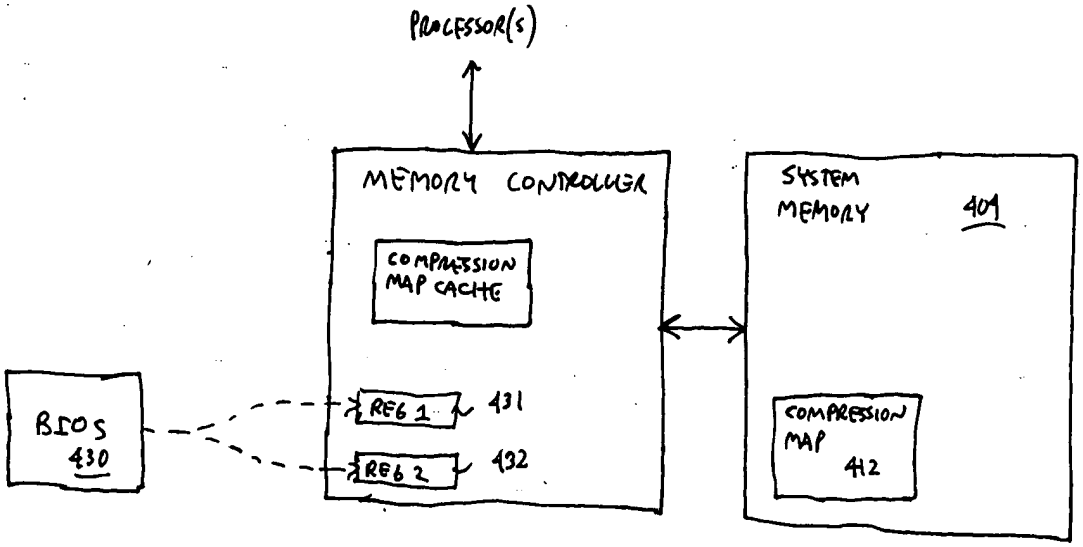

PROCESSOR(S)
MEMORY CONTROLLER
COMPRESSION MAP CACHE
REG 1
431
REG 2
432
BIOS
430
SYSTEM MEMORY
404
COMPRESSION MAP
412

FIG. 4D

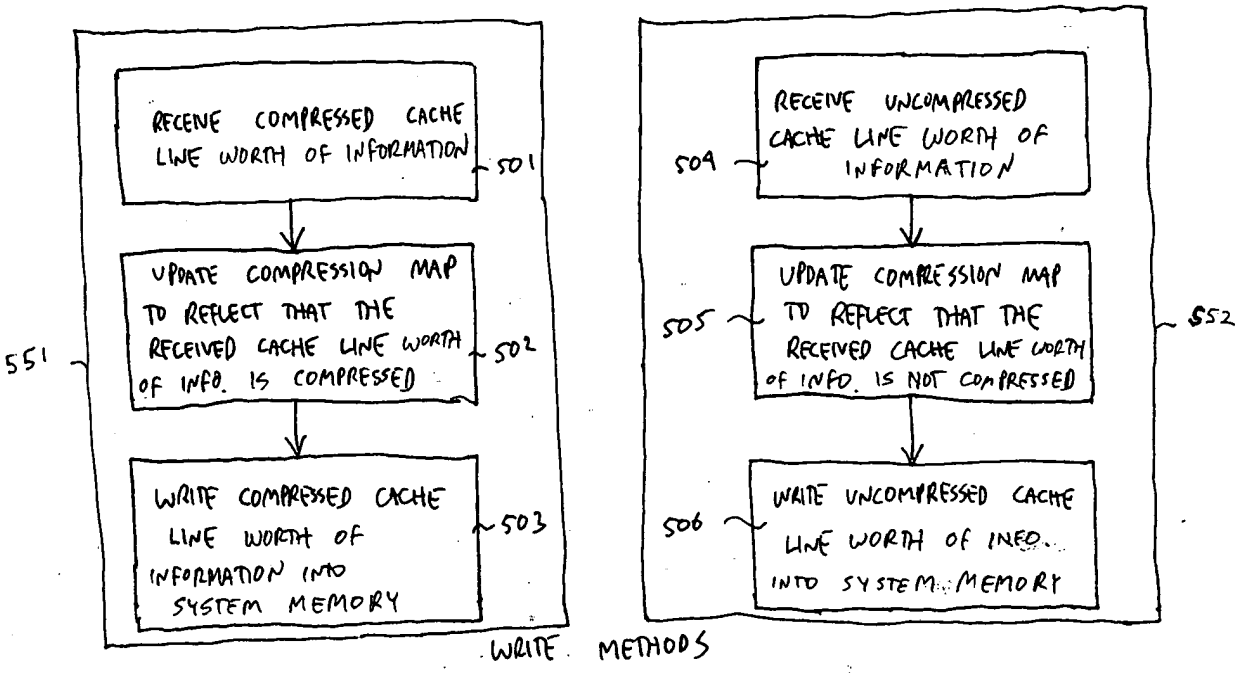
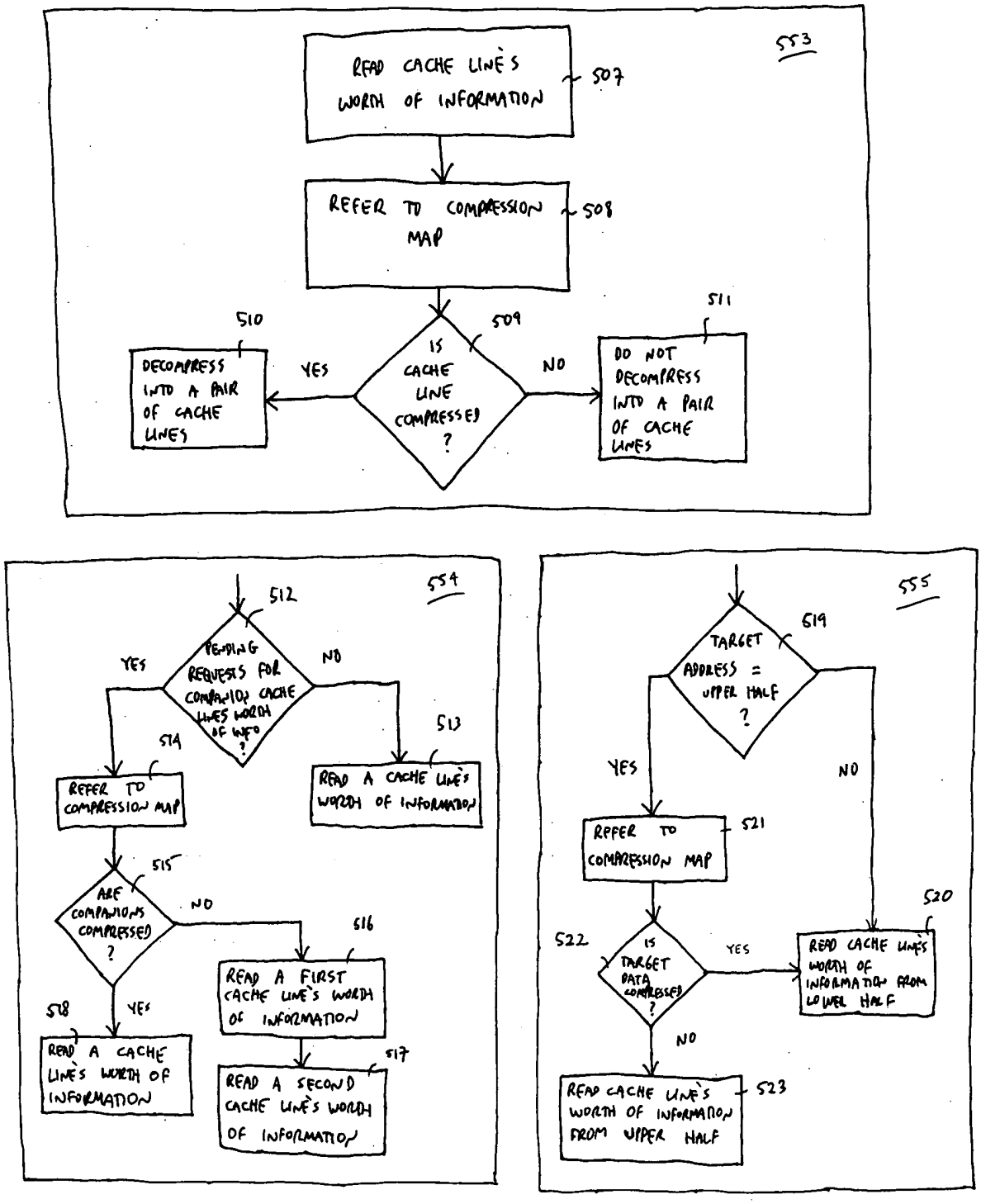

RECEIVE COMPRESSED CACHE LINE WORTH OF INFORMATION
501
UPDATE COMPRESSION MAP TO REFLECT THAT THE RECEIVED CACHE LINE WORTH OF INFO. IS COMPRESSED
502
WRITE COMPRESSED CACHE LINE WORTH OF INFORMATION INTO SYSTEM MEMORY
503
551
RECEIVE UNCOMPRESSED CACHE LINE WORTH OF INFORMATION
504
UPDATE COMPRESSION MAP TO REFLECT THAT THE RECEIVED CACHE LINE WORTH OF INFO. IS NOT COMPRESSED
505
WRITE UNCOMPRESSED CACHE LINE WORTH OF INFO. INTO SYSTEM MEMORY
506
552
WRITE METHODS

FIG. 5A



READ METHODS

FIG. 5B

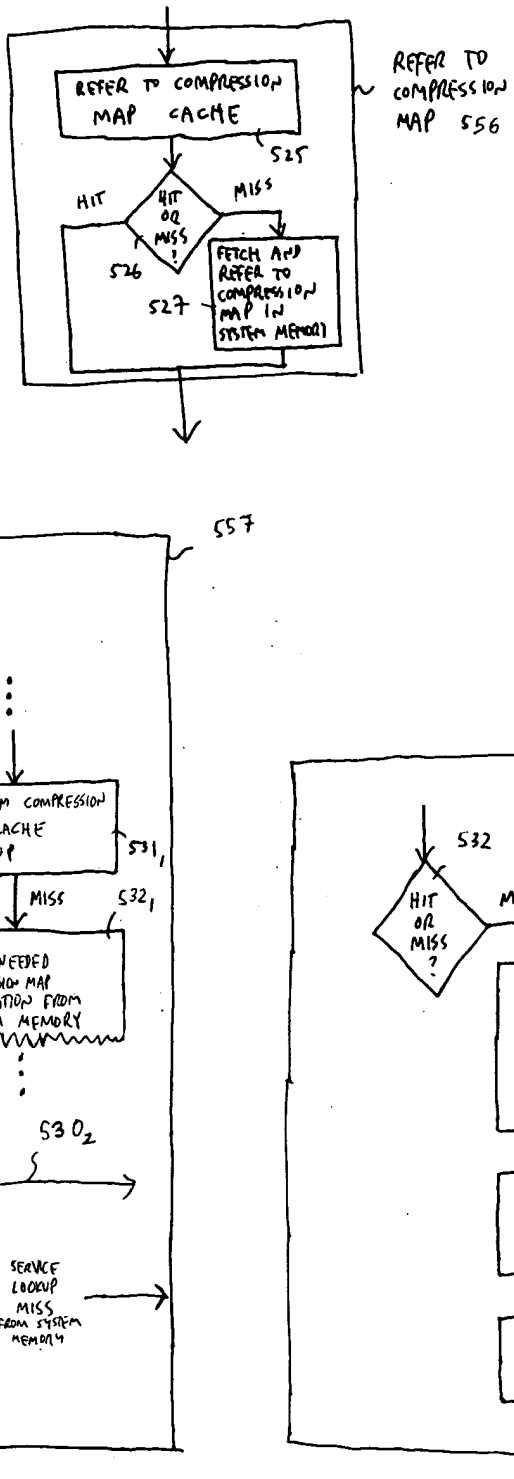

REFER TO COMPRESSION MAP CACHE
525
HIT OR MISS ?
HIT
MISS
526
FETCH AND REFER TO COMPRESSION MAP IN SYSTEM MEMORY
527
REFER TO COMPRESSION MAP 556
557
FETCH CACHE LINE'S WORTH OF INFORMATION FROM SYSTEM MEMORY
530_1
PERFORM COMPRESSION MAP CACHE LOOKUP
531_1
MISS
532_1
FETCH NEEDED COMPRESSION MAP INFORMATION FROM SYSTEM MEMORY
530_2
FETCH CACHE LINES WORTH OF INFORMATION FROM SYSTEM MEMORY
COMPRESSION MAP CACHE LOOKUP
SERVICE LOOKUP MISS FROM SYSTEM MEMORY
531_2
532_2
558
532
HIT OR MISS ?
MISS
533
READ CACHE LINES WORTH OF INFORMATION BASED ON A PREDICTED COMPRESSION/DECOMPRESSION STATE
534
FETCH COMPRESSION MAP FROM SYSTEM MEMORY
CHECK ACCURACY OF PREDICTION
535

FIG. 5C

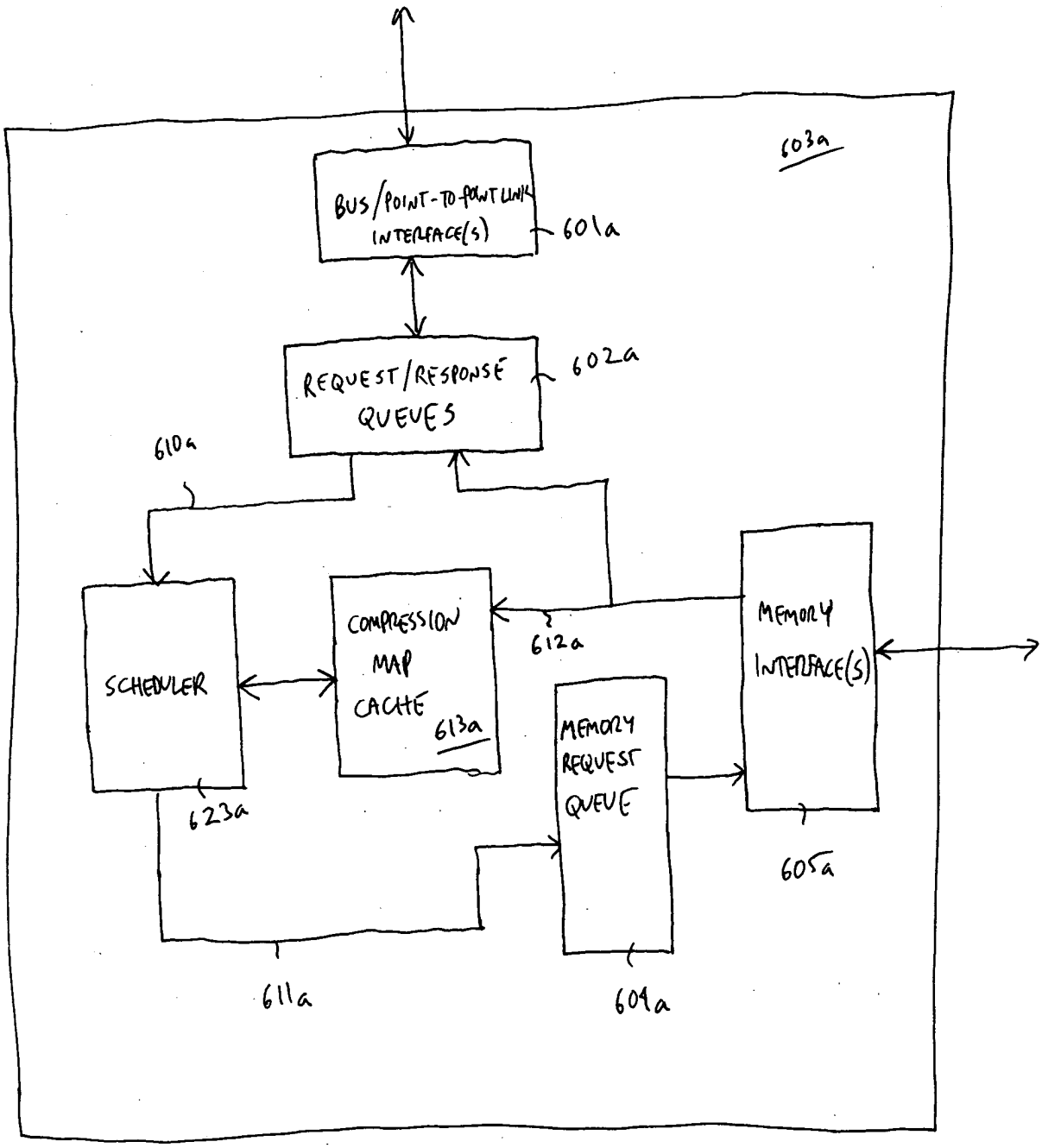

603a
BUS/POINT-TO-POINT LINK INTERFACE(S)
601a
REQUEST/RESPONSE QUEUES
602a
610a
SCHEDULER
COMPRESSION MAP CACHE
613a
612a
MEMORY INTERFACE(S)
623a
MEMORY REQUEST QUEUE
605a
611a
609a

FIG. 6A

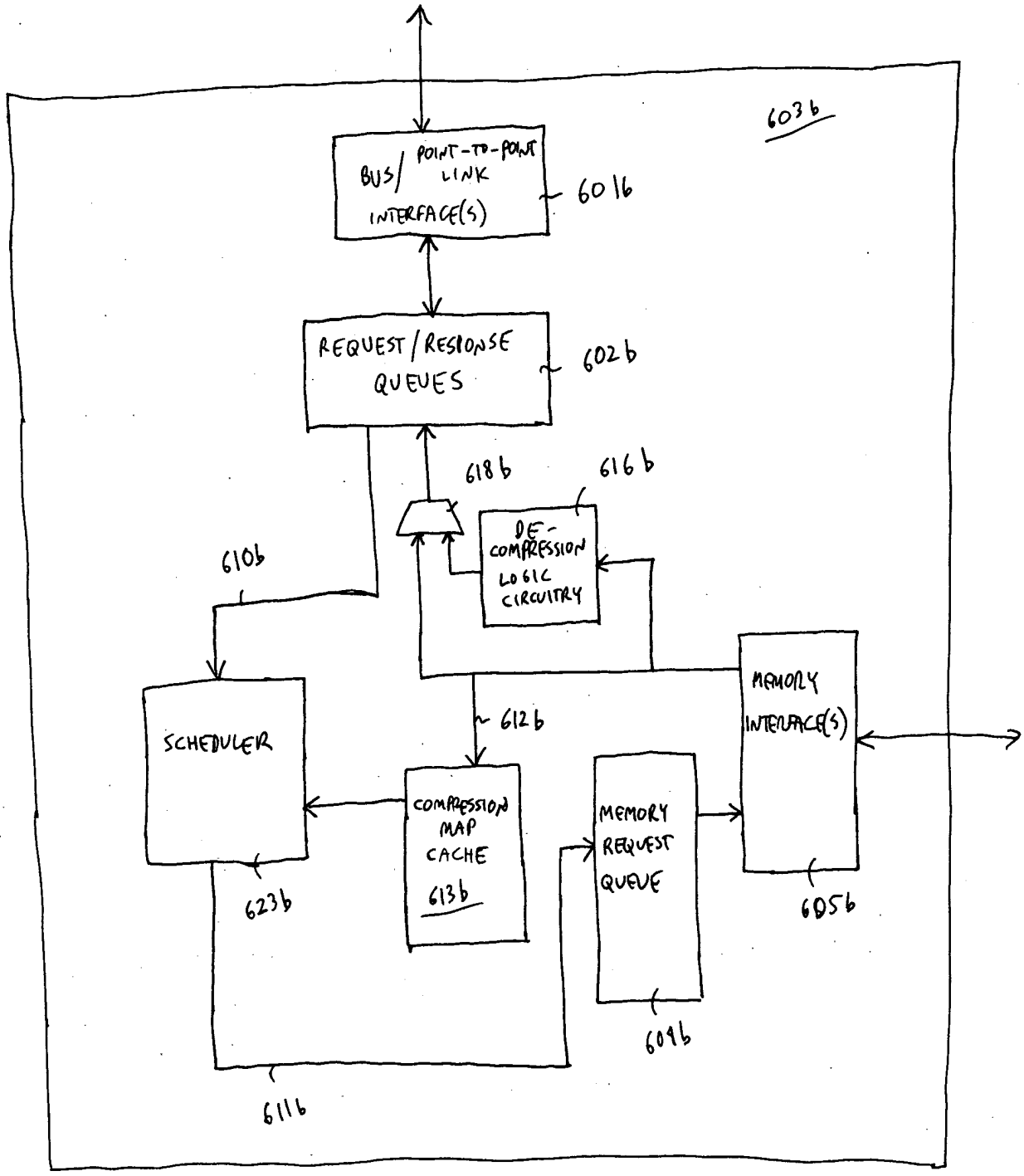

603b
BUS/ POINT-TO-POINT LINK INTERFACE(S)
601b
REQUEST/RESPONSE QUEUES
602b
618b
616b
DE-COMPRESSION LOGIC CIRCUITRY
610b
SCHEDULER
612b
MEMORY INTERFACE(S)
COMPRESSION MAP CACHE
613b
MEMORY REQUEST QUEUE
623b
605b
609b
611b

FIG. 6B

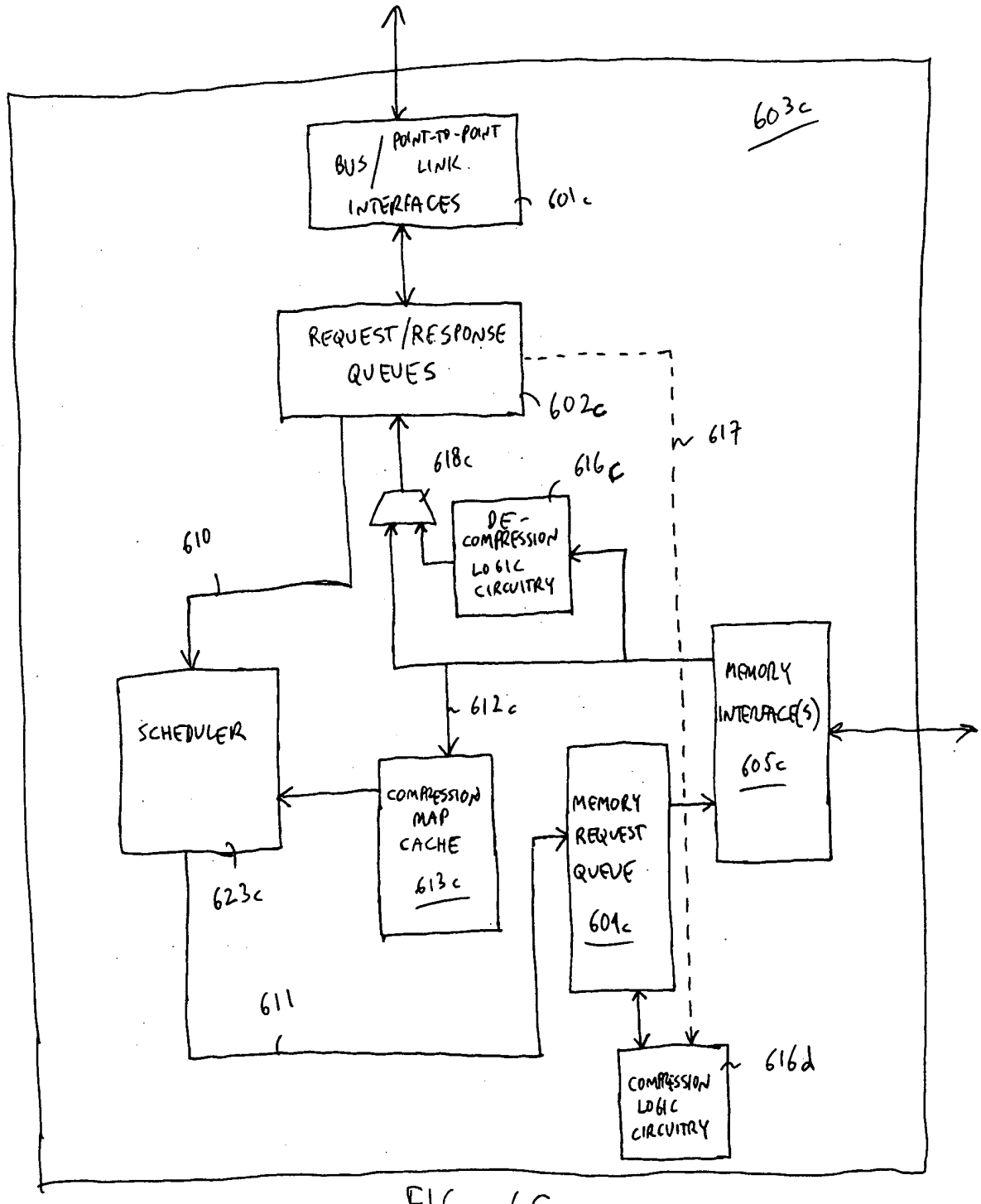

603c
BUS / POINT-TO-POINT LINK INTERFACES
601c
REQUEST/RESPONSE QUEUES
602c
617
618c
616c
DE-COMPRESSION LOGIC CIRCUITRY
610
SCHEDULER
612c
MEMORY INTERFACE(S)
605c
COMPRESSION MAP CACHE
613c
MEMORY REQUEST QUEUE
604c
623c
611
COMPRESSION LOGIC CIRCUITRY
616d

FIG. 6C

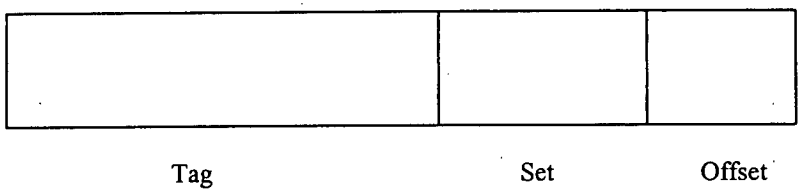


Figure 7A
(PRIOR ART)

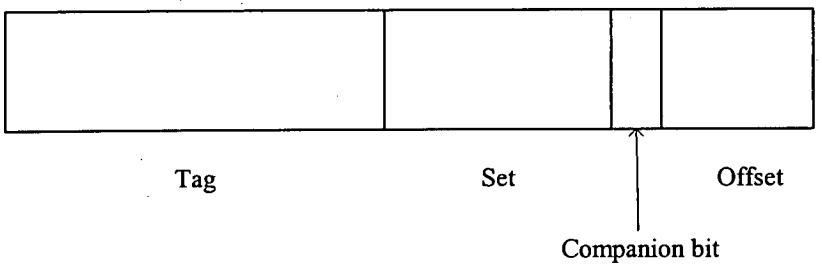


Figure 7B

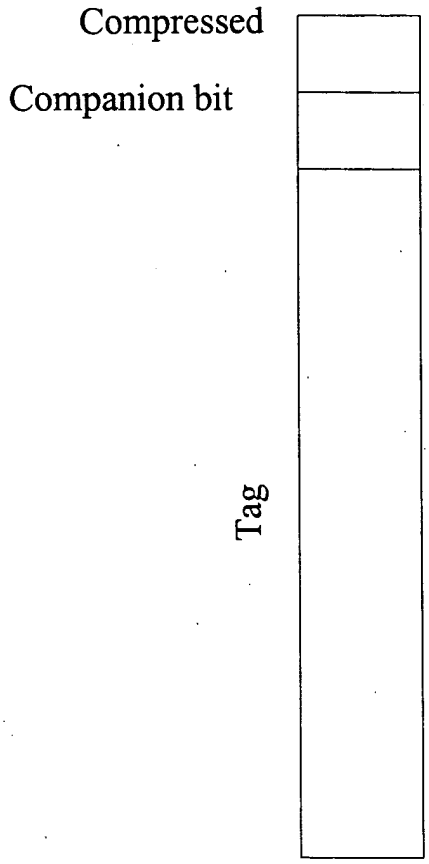


Figure 8

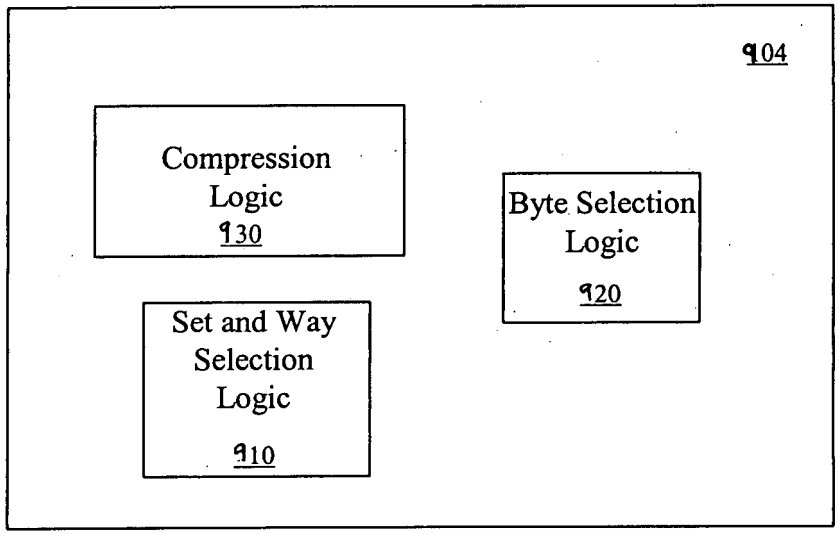

¶04
Compression Logic ¶30
Byte Selection Logic ¶20
Set and Way Selection Logic ¶10

Figure ¶

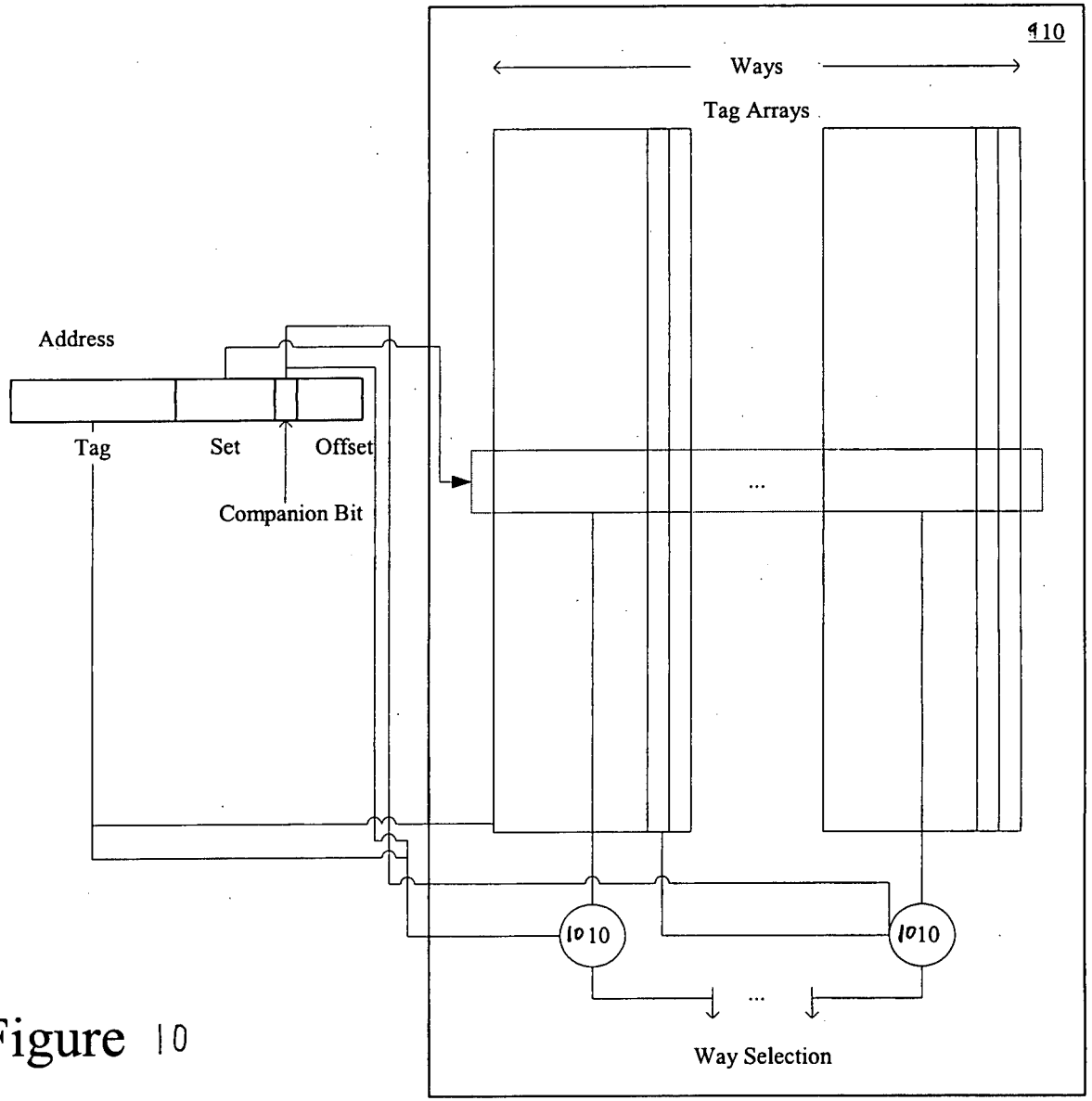

410
Ways
Tag Arrays
Address
Tag
Set
Offset
Companion Bit
...
1010
1010
...
Way Selection

Figure 10

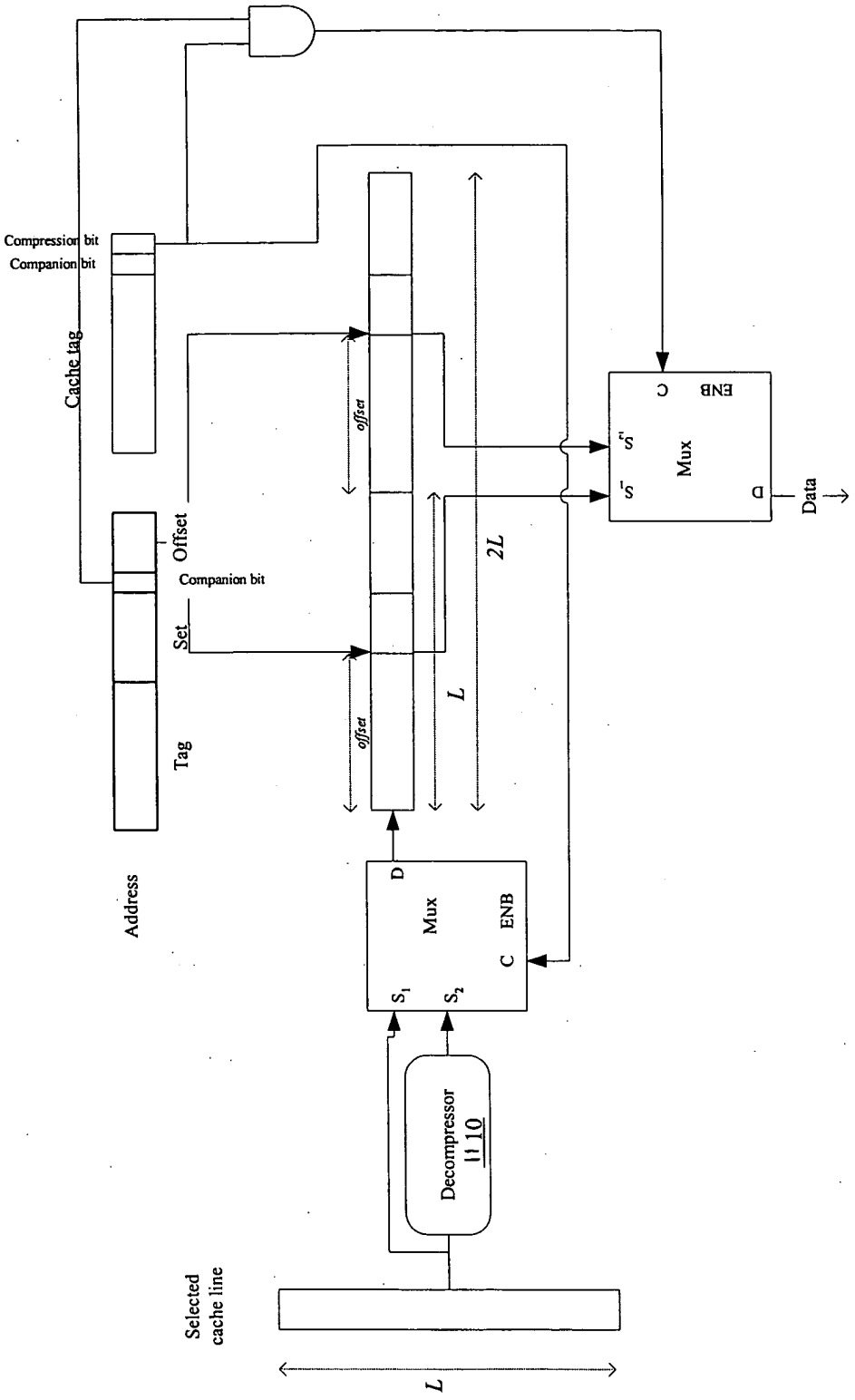

Compression bit
Companion bit
Cache tag
Offset
Companion bit
Set
Tag
Address
offset
offset
L
2L
Mux
ENB
C
D
S1
S2
Data
Decompressor
1110
Selected
cache line
L

Figure 11